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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN D. HYDE, MIGUEL E. FIGUEROA,
TODD E. HUMES, CHRISTOPHER J. DIORIO,
TERRY D. HASS, and CHAD A. LINDHORST

Appeal 2009-010687
Application 10/661,037
Technology Center 2800

Before JOHN C. MARTIN, JOSEPH F. RUGGIERO, and
BRADLEY W. BAUMEISTER, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF CASE

Summary

Claims 36-40 and 44-52 stand rejected under 35 U.S.C. § 103(a) over Bergemont (US 6,563,731 B1; issued May 13, 2003) in view of Yamashita (US 6,777,758 B2; issued Aug. 17, 2004). *See* App. Br. 14. Claims 1-35 and 41-43 have been canceled. App. Br. 5. Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of the pending claims.

We affirm.

Background and Analysis

"[Appellants'] invention relates to synapse transistors, as used for example in Digital-to-Analog Converters (DACs)." App. Br. 7. The synapse transistor is constructed of two devices – a readout transistor (such as a p-channel Field Effect Transistor) and a tunneling junction (such as a p-channel transistor that has the source and drain regions electrically shorted). *Id.* A floating gate, common to both the readout transistor and the tunneling junction, is formed over a tunnel oxide. App. Br. 7-8.

The rejection is based upon the Examiner's conclusion that it would have been obvious to have modified Bergemont's electrically erasable programmable read only memory (EEPROM) device depicted below:

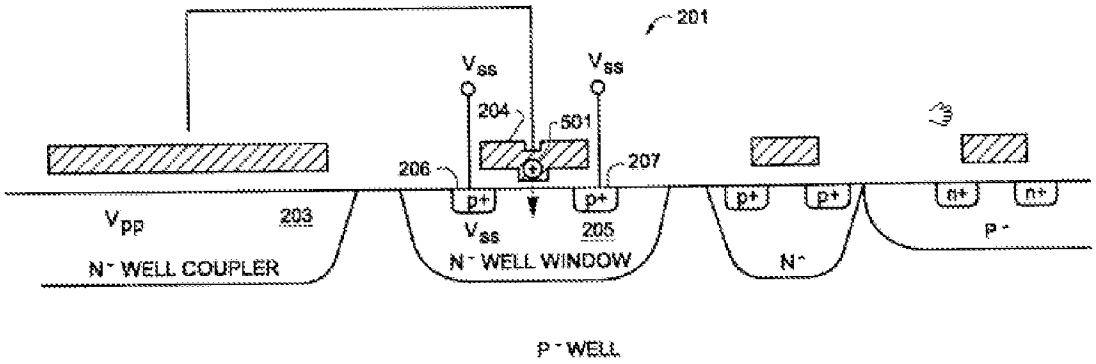

Figure 5 of Bergemont depicts an EEPROM cell 201 that is composed of an N-well coupler 203 and an N-well window transistor 205. EEPROM cell 201 is integrated with a pair of complementary metal oxide semiconductor (CMOS) transistors (unnumbered) within a common P-well.

More specifically, the Examiner initially found that it would have been obvious to have modified the combination of "a first n- well (to the *left* of well 205) [i.e., the N-well coupler] and second n- well 205 [i.e., the N-well window" (Ans. 3 (emphasis added)) by adding Yamashita's well contact terminal to the N-well window 205. Ans. 3-5.

Appellants argue two reasons for why such a modification would be improper.[2] We address these arguments separately.

Appellants first argue that Bergemont does not show the N-well coupler 203 having various claimed elements, and as such, "the

[2] Although Appellants nominally argue claims 38-40 and 50-52 separately from claims 36, 37, and 44-48 (App. Br. 15-17), the arguments presented for the former claims are substantially the same as those presented for the latter claims. Also, Appellants present no arguments with respect to claim 49 (*id.*), which depends from argued independent claim 48. Accordingly, we treat claims 36-40 and 44-52 as a single claim grouping, and we select claim 36 as representative of this group. *See* 37 C.F.R. § 41.37(c)(1)(vii).

interpretation that the Office Action seeks to take of Applicants' claims vis-à-vis Bergemont is fraught with inconsistencies and fails to account for all of [the] features set forth in the claims." App. Br. 15-16. Subsequently in the Examiner's Answer, though, the Examiner shifted the rejection's rationale, stating that the rejection is based upon the combination of the N-well window 205 and the transistor located to the *right* – not the left – of the N-well transistor. Ans. 6-7. Appellants have not filed a Reply Brief or otherwise responded to the Examiner's new rationale with any reasons for why the transistor to the right of the N-well window lacks any of the structures claimed. Accordingly, we understand the Examiner's finding regarding what structures Bergemont discloses to be uncontested.[3]

The only other issue raised on appeal, then, is whether it would have been obvious to have modified Bergemont's N-well window 205 to have further included a well contact terminal. Appellants have not disputed that the inclusion of a well contact terminal in such a manner would have been desirable or obvious from an operational standpoint. *See* App. Br. 15-17. Rather, Appellants only argue that the references are not combinable because, unlike Bergemont, Yamashita is not concerned with CMOS processing. App. Br. 16. Appellants conclude that the modification would "add tremendous costs to the fabrication, in direct contravention of the stated goals of Bergemont." *Id.*

However, Appellants do not set forth any evidence that adding a well contact terminal to Bergemont's N-well window 205 could not be performed

[3] Arguments which Appellants could have made but did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

using CMOS processing. *See Estee Lauder Inc. v. L'Oreal, S.A.*, 129 F.3d 588, 595 (Fed. Cir. 1997) ("[A]rguments of counsel cannot take the place of evidence lacking in the record."). Furthermore and to the contrary, Bergemont depicts the N-well window 205 already possessing source/drain contact terminals connecting to Vss. Fig. 5. We therefore do not see how adding an additional contact would require any processing that would be inconsistent with CMOS processing. "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

For the foregoing reasons, Appellants' arguments have not persuaded us of error in the Examiner's obviousness rejection of representative claim 36. Accordingly, we will sustain the Examiner's rejection of that claim as well as claims 37-40 and 44-52, which are grouped therewith.

DECISION

The Examiner's decision rejecting claims 36-40 and 44-52 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(v).

AFFIRMED

babc

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